

**UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION**

SOLAS OLED LTD.,

Plaintiff,

Case No. 6:19-cv-00236-ADA

v.

LG DISPLAY CO., LTD.,
LG ELECTRONICS, INC., and
SONY CORPORATION,

Defendants.

SOLAS'S RESPONSIVE CLAIM CONSTRUCTION BRIEF

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TABLE OF EXHIBITS AND ABBREVIATIONS

Ex ¹	Document Description	Abbreviation
1	Declaration of Richard A. Flasck in support of Solas's opening claim construction brief	Flasck. Decl.
2	U.S. Patent No. 7,907,137	'137 patent
3	U.S. Patent No. 7,432,891	'891 patent
4	U.S. Patent No. 7,573,068	'068 patent
5	Parties' joint revised list of terms/constructions dated March 6, 2020	Joint Chart
6	Microsoft Computer Dictionary (3rd ed., 1997), definition of "signal"	MS Dict.
7	McGraw-Hill Dictionary of Scientific and Technical Terms (4th ed., 1989), definition of "data transmission line"	McGraw-Hill
8	Merriam-Webster Dictionary (avail. at www.merriam-webster.com , accessed Feb 2020), definitions of "along" and "together"	Merriam-Webster
9	Dictionary.com (avail. at www.dictionary.com , accessed Feb. 2020), definitions of "along" and "together"	Dictionary.com
10	Defendant LG Display's petition for <i>inter partes</i> review in IPR2020-00177 on the '891 patent	'891 IPR Pet.
11	Defendant LG Display's expert declaration by Dr. Hatalis in <i>inter partes review</i> in IPR2020-00177 on the '891 patent	'891 IPR Decl.
12	U.S. Patent No. 5,106,652	'652 patent
13	U.S. Patent No. 5,981,317	'317 patent
14	U.S. Patent Appl. Pub. No. 2002/0101172	'173 app. pub.
15	U.S. Patent No. 7,250,722	'722 patent
16	Declaration of Richard A. Flasck in support of Solas's responsive claim construction brief	Flasck Resp. Decl.
17	US Patent App. Pub. 2004/0239596	Ono
	Declaration of Douglas R. Holberg in support of Defendants' opening claim construction brief (Dkt. 67-2)	Holberg Decl.

¹ Exhibits 1–15 submitted with Solas's opening claim construction brief (Dkt. 68-2 to 68-16). Exhibits 16–17 are attached to this brief.

I. DISPUTED TERMS FOR '137 PATENT

A. “a gradation current having a current value” ('137 patent claims 10, 36)

Solas's Proposed Construction	Defendants' Proposed Construction
a current having a current value and conveying information about a level	an actual current <u>(not voltage) with a value</u> corresponding to a luminance level

Defendants' brief attacks a strawman. This term requires that there be a current, and Solas's construction fully acknowledges that. *See* Flasck Resp. Decl. ¶¶ 2–8. As both sides recognize, a current is a physical quantity with a broadly accepted meaning. Both sides agree that a current, in the context of the '137 patent, is a “flow of electric charge.” Defs.' Br. at 2; Flasck Decl., at ¶ 31. Indeed, both sides cite the same dictionary definition for current:

current \kur'ənt\ *n.* The flow of electric charge through a conductor, or the amount of such flow. Current is measured in amperes. *See also* ampere, coulomb. *Compare* volt.

Microsoft Computer Dictionary (1997), Dkt. 67, Ex. 4; *see* Flasck Decl., Dkt. 68, Ex. 1, ¶ 66. But Defendants' construction does not attempt to define current. Rather, they attempts to exclude things that in fact meet the commonly used definition of current from the scope of this term.

Contrary to the assertions in Defendants' opening brief, Solas does not view voltage and current as “interchangeable synonyms.” Defs. Br., Dkt. 67 at 6. Solas enthusiastically agrees that current and voltage are well-defined, distinct electrical phenomena. And Solas has no plan to point to some different type of physical quantity, such as voltage, mass, capacitance, magnetic field, or temperature, and call that other physical quantity a current.

Nevertheless, Defendants' proposed parenthetical “(not voltage)” invites reversible legal error. Defendants have not shown any disclaimer, let alone one that needlessly requires the

negative limitation they seek to import. And, to make matters worse, that negative limitation here concerns an inextricably intertwined electrical phenomena.

It is undisputed that current and voltage are inextricable intertwined. Indeed, the intrinsic and extrinsic record are one-sided on this fact. As just one example, Defendants conspicuously did not obtain or present any expert opinions about a POSITA viewpoint on this issue.

Despite not presenting any such evidence, Defendants still cannot avoid the well-established fact that the two phenomena are so intertwined. Both sides used an analogy of water flowing through a pipe or hose in explaining the concepts of current and voltage in their opening submissions. Defs.’ Br., Dkt. 67 at 2–3; Flasck Decl., Dkt. 68, Ex. 1, ¶¶ 30–34. As Defendants presented the analogy, “[c]urrent is like the rate at which the water flows, and voltage is like the water pressure that forces the water through the pipe.” Defs.’ Br., Dkt. 67 at 2–3. In the pipe, when you take away the pressure, the flow stops. In an analogous manner, current and voltage in a circuit are interconnected. As Defendants’ expert explains, “[v]oltage’ is the potential energy required to move electrons from one point to another in a circuit,” i.e., it provides the energy needed to make a current flow. Holberg Decl., Dkt. 67, Ex. 1, ¶ 26.

This connection between the gradation current and voltages is described explicitly in the specification. The gradation current is generated within the gradation signal generation unit from a voltage using a “voltage-current converter.” ’137 patent at 10:45–11:3. This current supplies the electric charges to charge the capacitor with “the voltage component V_{data} appropriately corresponding to the gradation signal (display data),” providing a “current/voltage conversion function.” *Id.* at 22:37–54, 24:38–39. The result of this process is a “gradation voltage” that is applied to the gate of the drive transistor. *Id.* at 2:49–52, 11:4–13.

The claim as written requires a current. Defendants seek to add a new requirement, that there not also be a voltage present. By analogy, they seek to require that the water flow from the pipe even though the pressure is turned off. Even if a current without a voltage were physically possible, such a construction would improperly exclude the preferred embodiments, which utilize both currents and voltages together in delivering signals that control pixel brightness.

None of the cases cited by Defendants supports the negative limitations they seek to include here. *Cave Consulting* does not endorse the use of negative limitations in claim constructions at all. *Cave Consulting Group, LLC v. OptumInsight, Inc.*, 725 Fed. Appx. 988, 990 (Fed. Cir. 2018) (unpublished). In that case, neither party proposed a construction with a negative limitation, and the district court did not adopt such a construction. *Id.* at 990. In reversing the district court, the Federal Circuit did not adopt any explicit construction, but simply held that when properly construed the claims did not encompass a certain category of embodiments. *Id.* at 995–96.

In *Symantec*, the effect of the court’s construction was to define the claim term “normal” as “typical attack-free.” *Trustees of Columbia U. in City of New York v. Symantec Corp.*, 811 F.3d 1359, 1368 (Fed. Cir. 2016). This construction was based on clear statements in the specification equating “normal” with “free of attacks.” *Id.* Likewise, the court’s construction in *Mangosoft* actually defined the term “migrate” based upon how the term was used in the specification. *Mangosoft Intell. Prop., Inc. v. Skype Techs. SA*, CIV. A. 2:06-CV-390, 2008 WL 3852740, at *7 (E.D. Tex. Aug. 14, 2008). In neither case did the court insert extraneous negative limitations into terms with undisputed plain and ordinary meaning, as Defendants seek to do here.

In both *RFID* and *Computer Docking Station*, the Federal Circuit did endorse a negative limitation. But in each case, the negative limitation was based on a “clear and unmistakable” disclaimer of scope due to statements made during prosecution to distinguish prior art. *RFID*

Tracker, Ltd. v. Wal-Mart Stores, Inc., 342 Fed. Appx. 628, 631–32 (Fed. Cir. 2009) (unpublished)); *Computer Docking Station v. Dell*, 519 F.3d 1366, 1375–76 (Fed. Cir. 2008).

Defendants suggest that the patentee disavowed any use of voltages during prosecution. But the statements cited by Defendants concerning voltages do not meet the “clear and unambiguous” standard required for prosecution disclaimers. *Contl. Circuits LLC v. Intel Corp.*, 915 F.3d 788, 798 (Fed. Cir. 2019) (“the statement in the prosecution history must be clear and unambiguous, and constitute a clear disavowal of scope”). The amendment that Defendants point to added a requirement of a “gradation current having a current value.” Dkt. 67, Ex. 5 at 2. It said nothing whatsoever about voltages.

As for the statements during prosecution distinguishing the Ono prior art reference, Defendants quote statements from two different paragraphs. In the first of these paragraphs, the applicant described disclosures from Ono and specifically calls out three voltages used in Ono: the “data voltage,” the “threshold voltage,” and the voltage obtained by adding these two voltages. Dkt. 67, Ex. 7 at 32. In the other paragraph, the applicant distinguished Ono, explaining that Ono “does not disclose generating a supplying a gradation current as a gradation signal.” *Id.* The natural reading of these two paragraphs is that none of the voltages disclosed in Ono is a “gradation current” (due to the uncontroversial fact that a voltage is not a current) and that claim 1 as amended required a “gradation current” (likewise uncontroversial). No narrowing of the claims is suggested by these statements during prosecution beyond what is already explicit in the claims. Nothing in these statements suggests that the claims would not cover an embodiment that contained a gradation current but also contained one or more voltages. And even if such a suggestions could be discerned in the prosecution history, these statements do not meet the standard of “clear and unambiguous” disavowal of such embodiments from the claims.

Defendants also suggest that Solas’s construction “would create needless ambiguity” (Dkt. 67 at 5), but it is Defendants’ construction that introduces ambiguity. Defendants’ use of the word “actual” appears to suggest that some currents are “actual currents” and that other currents fall short of that lofty designation. But neither Defendants’ opening brief nor the intrinsic record supports this distinction or explains what sort of entity could be a “current” (as in Solas’s construction), but not also be an “actual current” (as in Defendants’ construction). Under Defendants’ construction, the jurors will be left to speculate at what “false currents,” “almost currents,” “partial currents,” or “just-barely currents” are meant to fall outside the scope of “actual current.” But in their speculation, the jurors will be left with the unmistakable impression that the Court put its thumb on the scale and instructed them that “current” in the claims has some special meaning, which excludes things that would otherwise fall within the scope of the term “current.” In construing the term in this manner, the Court would needlessly invite error.

“Current” has a clear and undisputed meaning. This term requires that there be a current that meets the requirements of the limitation—nothing more. Defendants’ efforts to limit the claims by excluding currents that meet the plain meaning of this term are unsupported by the record, invite confusion and error, and should be rejected.

B. “gradation signal” (’137 patent claims 10, 15, 36, 37, 39)

Solas’s Proposed Construction	Defendants’ Proposed Construction
signal conveying information about a level	a gradation <u>current with a current value sent to a pixel to set a luminance gradation</u>

Defendants’ proposed construction wrongly attempts to distort the well understood term “signal” with a lengthy and incorrect construction. But Defendants provide no justification for construing the well understood claim term at all—and certainly no reason for construing it in the way that they want: replacing it with *fourteen different words* of their choosing.

Defendants do not dispute that the term “signal” has a plain meaning. As the intrinsic and extrinsic record make obvious, of course it does. And Defendants also do not—and could not—argue that the patentee disclaimed from that well understood plain meaning or that the patentee acted as his own lexicographer in defining it in his own way. These established points alone are dispositive: the term “signal” needs no further construction. Rather, where a term is used in accordance with its plain meaning, the court should not replace it with different language. *Thorner v. Sony Computer Ent. Am. LLC*, 669 F.3d 1362, 1366-67 (Fed. Cir. 2012) (“we do not redefine words. Only the patentee can do that.”).

Even if the claim term “signal” did need to be replaced, Defendants’ proposed replacement would lead to reversible error. Defendants’ construction incorrectly requires that the “gradation signal” *always must* be a “gradation current” and have a “current value.” But that contradicts the intrinsic record and *excludes* embodiments.

On the patent specification, Defendants’ proposal contradicts the numerous examples of “gradation signals” that are “non-light emitting display *voltages*” cited in Solas’s opening brief. Defendants proposal would exclude all this. *See* Flasck Decl. ¶¶ 72–73. Such constructions are “rarely, if ever, correct.” *SanDisk Corp. v. Memorex Prod., Inc.*, 415 F.3d 1278, 1285 (Fed. Cir. 2005). And for their part, Defendants provide no intrinsic or expert testimony that would ever suggest that a POSITA would view this disputed term as one of the “rarely, if ever, correct” scenarios in which to apply this exclusion.

On the claims, though they require generating and/or supplying “a gradation current . . . as a gradation signal.” ’137 patent at 58:5–12, 62:55–60, that does not mean that a “gradation signal” as used in the ’137 patent *can only ever be* a gradation current. If anything, that language suggests the opposite, because if a “gradation signal” is necessarily a “gradation current,” there would be

no reason to use both terms in the same claims. And Defendants’ proposal outright contradicts dependent claims, which, consistent with the specification, makes clear that a gradation signal can also be “a voltage.” *See* ’137 cl. 15, 39.

Solas’s proposal, on the other hand, properly explains the plain meaning of this term, in the context of the patent and claims—and does so consistent with the parties’ agreement on other terms. The parties agree that “**luminance gradation**” means “**light-emitting level**.” Solas’s construction is consistent with this—and only helps the fact-finder better understand “gradation” as it is used in the “gradation signals” taught in the patent. Flasck Decl. ¶¶ 63–73.

Instead of providing any valid reason for construing that claim term, let alone construing it in the overly narrow and distorted manner they seek, Defendants wrongly accuse Solas of “ignor[ing]” surrounding claim language “generates a gradation current having a current value.” Defs.’ Br., Dkt. 67 at 9. But even accepting this premise and ignoring the numerous defects in their proposal, Defendants’ argument only confirms that no construction is necessary. The claim term Defendants proposed construing is “gradation signal”—not the larger claim phrase—and their proposed construction merely seeks to replace the single claim term “signal.” If the surrounding language actually imposes the requirement that Defendants suggest, then there is no need to redundantly burden the construction of “gradation signal” with that requirement as well. *US Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997) (claim construction is “*not* an obligatory exercise in redundancy.”).²

At best, Defendants’ proposal is unhelpful. It incorporates by paraphrase requirements that appear elsewhere in the claims such as the requirement that the “gradation current” be “supplie[d] . . . to the display pixel” or that it be related to the “luminance gradation.” ’137 patent at 58:9–12.

² All emphasis added unless otherwise noted.

This is unnecessary and confusing. And again, at worst, their proposal actually excludes embodiments and creates tension with other parts of the intrinsic record, including the actual claim language of dependent claims. Either way, it must fail. And as Defendants make clear with the next “dispute” they raise, they appear to present their baseless and incorrect attorney argument on this claim construction dispute to prop up another incorrect attorney argument on the next dispute.

C. **“generates, as the gradation signal, a non-light emitting display voltage ...”**
(’137 patent claim 15) “a non-light emitting display voltage ...is generated as the gradation signal (’137 patent claim 39)

Under controlling law, a claim is only invalid as indefinite if, when read in light of the specification and prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention. *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 898–899 (2014). Defendants bear the burden of proving this defense by clear and convincing *evidence*. *BASF Corp. v. Johnson Matthey, Inc.*, 875 F.3d 1360, 1365 (Fed. Cir. 2017).

But LG provides *no evidence* to meet its burden. Though given the opportunity, it provides no testimony that a POSITA, with the patent and file history in hand, could not make any sense of these dependent claims, as Defendants contend. It provides *no* other credible evidence to support this incredible position, either. This stands in contrast to the considerable intrinsic and extrinsic evidence provided by Solas. For example, Dr. Flasck’s testimony alone makes clear that, a POSITA would immediately and easily understand the scope of dependent 15 and 39 in light of the intrinsic record, precisely as Solas contends. *See, e.g.*, Flasck Decl. ¶¶ 74–81.

Because Defendants bear a heavy burden on this indefiniteness defense, which involves underlying factual questions, these facts alone is dispositive. The law on this point is straightforward. For example, in *Apple, Inc. v. Samsung Elecs. Co. Ltd.*, the Federal Circuit found that Samsung points to no evidence showing the skilled artisans would find [the disputed element]

as lacking reasonable certainty in its scope. In contrast, Apple’s expert explained that [the] patent provides skilled artisans with enough information to understand what [the disputed element] means in the patent.” 786 F.3d 983, 1003 (Fed. Cir. 2015). Thus, the court held that district court was correct in holding that “Samsung failed to carry its burden [on] indefiniteness,” even if the issue concerned claim construction disputes. District courts have followed this approach as well. *Fisher-Rosemount Systems, Inc. v. ABB Ltd.*, Civ. No. 4:18-CV-00178, 2019 WL 6830806, at *10-11 (S.D. Tex. December 12, 2019) (“patents are not addressed to lawyers, or even to the public generally, but rather to those skilled in the relevant art”—and relying on patentee’s expert testimony on how those skilled in art would understand the term to deny defendant’s summary judgment of indefiniteness); *f’real foods, LLC v. Hamilton Beach Brands, Inc.*, Civ. No. 16-41-CFC, 2019 WL 1648411, at *2 (D. Del. April 16, 2019); (denying summary judgment of indefiniteness because patentee’s technical expert raised an issue of fact.)

Instead of providing any convincing evidence, Defendants admittedly only piggyback on their brief, yet fatally flawed, attorney argument that “gradation signal” must be construed as “gradation current.” Defs’ Br. at 9-10 (The [indefiniteness] dispute here rises and falls with the construction of ‘gradation signal.’”). But that fails for the same reasons their construction of “gradation signal” fails. And it is no substitute for clear and convincing evidence in any event.

Indeed, even ignoring Solas’s expert, the intrinsic record alone also confirms Defendants could not meet their burden even, if they had tried much harder and actually presented meaningful evidence. That is because the intrinsic and other extrinsic evidence makes clear that Defendants’ defense has several fundamental and fatal defects as explained in Solas’s opening brief. *See* Br. at 10–13 (discussing the teachings of patent specification, figures, claims, and dependent claims). This evidence demonstrates and Defendants’ indefiniteness assertion must fail.

This evidence stand in sharp contrast to the single substantive case on which Defendants rely, the decades-old *Process Control* decision, which merely stood for the unremarkable proposition that where “claims are susceptible to *only one reasonable interpretation and that interpretation results in a nonsensical* construction of the claim as a whole, the claim must be invalidated.” *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357 (Fed. Cir. 1999). Here, the exact opposite is true: there is only one reasonable construction: it is Solas’s construction, *not* Defendants’ tortured construction.

D. “through a data line . . . through the data line . . . through the data line” (’137 patent claims 10, 16)

Solas’s Proposed Construction	Defendants’ Proposed Construction
plain and ordinary meaning. “a data line” means “one or more data lines.” The antecedent basis for “the data line” is “a data line.”	the gradation current is supplied, the threshold voltage is detected, and the compensation voltage is applied through the same data line

The parties present a legal dispute about the meaning of “a data line” and “the data line.” As to “a data line,” the indefinite article “a” in patent parlance means “one or more.” *See* Br. at 14 (quoting *KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1356 (Fed. Cir. 2000)). “That ‘a’ or ‘an’ can mean ‘one or more’ is best described as a **rule**, rather than merely as a presumption or even a convention.” *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1342 (Fed. Cir. 2008). Defendants acknowledge this and appear to agree that “a data line” means “one or more data lines.” *See* Defs.’ Br. at 11.

As to “the data line,” it takes antecedent basis from the earlier term “a data line.” But this does not imply a singular data line. Rather: “The use of definite articles ‘the’ or ‘said’ in a claim to refer back to the same claim term does not change the **general plural rule**, but simply **reinvokes that non-singular meaning**.” *Baldwin* at 1342–43 (where a claim element may be plural, a later reference to that same element “does not alter that meaning in the slightest”).

Defendants seek an exception to the established rule by requiring all “data line” terms to refer to “the same *singular* data line.” *See* Defs.’ Br. at 12. But such exceptions are “extremely limited: a patentee must ‘evince a *clear intent*’” to limit the term to the singular. *Baldwin* at 1342. And Defendants are required to show that “the language of the claims themselves, the specification, or the prosecution history necessitate a departure from the rule.” *Id.* at 1342–1343.

Here, Defendants make no showing based on the claims or specification. Neither the claims nor the specification require the recited functions be performed through the same, singular data line. For example, there is no reason the gradation current cannot be supplied through two data lines and the voltage is detected and applied through one or more of those data lines.

In similar circumstances, courts have held multiple recited functions need not be performed by a single element. In *Elkay Mfg. v. Ebco Mfg. C.*, the Federal Circuit held that the plain meaning of a claim that recited a feed tube to provide a flow path for delivering liquid and admitting air “is not limited to a single feed tube with a single flow path for both liquid and air.” 192 F.3d 973, 977 (Fed. Cir. 1999). And in *Freeny v. Fossil Group*, the Eastern District held that multiple instances of “the request authorization code” did not require construction and is not limited to “the *same* request authorization code.” Case No. 2:18-CV-00049-JRG-RSP, 2019 WL 2078783, at *12–16 (E.D. Tex. May 10, 2019). As the court explained, “when the claim refers to outputting ‘the request authorization code’ on a first signal, and outputting ‘the request authorization code’ on a second signal, that language means that any of the ‘one or more request authorization codes’ can be outputted on the first and second signals to satisfy the claim.” *Id.* at *14.

As to the prosecution history, Defendants fail to show disclaimer. In response to an anticipation rejection, the applicants distinguished Ono as disclosing detecting a threshold voltage based on “**grounding** line 6”—as opposed to a “data line.” Defs.’ Ex. 7 at 32; *see also* Ono at Fig.

1, [0027] (distinguishing “grounding conductor 6” from “data line 7,” and never characterizing the grounding conductor as a data line). The applicants never disclaimed the possibility that supplying, applying, and detecting could be performed through different data lines. This is not clear and unmistakable disclaimer. *See Golight, Inc. v. Wal-Mart Stores, Inc.*, 355 F.3d 1327, 1332 (Fed. Cir. 2004) (where “statements in the prosecution history are subject to multiple reasonable interpretations, they do not constitute a clear and unmistakable” disclaimer). *Core Wireless v. LG Elec., Inc.*, 880 F.3d 1356, 1367 (Fed. Cir. 2018) (same).

Defendants’ cited cases are inapposite and do not support its argument. These cases were all discussed and distinguished in *Freeny v. Fossil Group* above, where the Eastern rejected a similar argument to one Defendants now make. *See* 2019 WL 2078783, at *16. In *In re Varma*, the court held that the claim limitation “a statistical analysis request corresponding to two or more selected investments” could not be met by two separate requests where each request has just one selected investment. 816 F.3d 1352 at 1362–63. This is the plain reading of the “corresponding to” language in the claim. *See id.* No such language exist in the claims here. Likewise in *Plano Encryption Techs., LLC v. Alkami, Inc.*, the court construed “a storage medium having stored therein a plurality of programming instructions” to mean just one storage medium storing the instructions. 2:16-cv-01032, Dkt. 168, 2017 WL 3654122, at *18–22 (E.D. Tex. Aug. 23, 2017). Again, this is a plain reading of “having stored therein.” No such limiting language exists in the claims here. Finally, in *TiVo Inc. v. EchoStar Commc’ns Corp.*, the court construed “assembl[ing] said video and audio components into an MPEG stream” to mean assembling those components into only one stream because the patent specification required it. 516 F.3d 1290, 1303–04 (Fed. Cir. 2008). Here, there is nothing in the specification that requires the supplying, applying, and detecting functions to be on the same, singular data line.

E. “before” (‘137 patent claim 10) / “after” (‘137 patent claim 36)

Term	Solas’s Proposed Construction	Defendants’ Proposed Construction
“before”	plain and ordinary meaning	earlier in time (not at the same time)
“after”	plain and ordinary meaning	later in time (not at the same time)

The Court is not required to construe the simple words “before” and “after.” As the Federal Circuit instructed, “there are limits to the court’s duties at the claim construction stage. For example, courts should not resolve questions that do not go to claim scope, but instead go to infringement, or improper attorney argument.” *Eon Corp. IP Holdings v. Silver Spring Networks*, 815 F.3d 1314, 1319 (Fed. Cir. 2016). Indeed, “district courts are not (and should not be) required to construe every limitation present in a patent’s asserted claims.” *O2 Micro Int’l v. Beyond Innovation Tech.* 521 F.3d 1351, 1362 (Fed. Cir. 2008).

“Before” and “after” are plain English words and easily understood by the jury. Defendants do not suggest otherwise. Nor do Defendants explain how their constructions differ from these words or what additional clarification they provide. Thus, Defendants’ constructions are at best redundant, and will likely introduce confusion and ambiguity.

In arguing for their constructions, Defendants imply they will say their constructions really mean “*without any overlap in time.*” See Defs.’ Br. at 13. This shadow construction should be rejected for several reasons. *First*, Defendants did not propose “without any overlap in time” as part of their constructions. Having made that choice, Defendants should not be allowed to re-interpret their constructions or argue they have a different, particular meaning. *Second*, “without any overlap in time” is not the plain and ordinary meaning of “before” and “after.” Defendants cite four dictionary definitions (Defs.’ Br. at 13, n. 11), and none of them mention “overlap” or “without any overlap in time.” And in the context of electronic circuits, a POSITA would not

understand that “before” requires a first process to begin and *entirely complete* before a second process begins. *See* Flasck Decl. ¶ 86. Rather, a POSITA consider the amount of time overlap and other factors such as the causal relationship between the two processes. *See id.*

Third, Defendants do not identify any disclaimer or lexicography that mandates “without any overlap in time.” Defendants’ points to an alleged example in the specification, but it is improper to import examples or embodiments into the claims. Nor does the prosecution history show the requisite disclaimer. Nowhere does the prosecution history mention the words “overlap” or “without any overlap in time.” Instead, during prosecution the applicants unremarkably explained that “applies . . . before” means “previously applied.” Defs’ Ex. 7 at 28.

The applicants also contrasted a reference where the compensated gradation voltage was “generated” and “supplied” in exactly the same step: by adding a gradation voltage and a compensation voltage. *Id.* at 29, 32. Therefore, in this reference, by definition the “generating” and “supplying” occurred at exactly the same time. The applicants explained that this aspect of the reference, which suggested *complete* overlap in time, does not meet the claim terms “before” and “after.” At most, the applicant disclaimed two processes that occur at exactly the same time, which is already apparent from the plain meanings of “before” and “after.” There was no clear and unmistakable disclaimer to support Defendants’ extreme narrowing of these terms.

II. DISPUTED TERMS FOR ’891 PATENT

A. “a third thin film transistor ...” (’891 patent claims 1, 3)

To supports their narrowing construction, Defendants rely almost entirely on the claim language. Defs.’ Br. at 17–18. But nowhere does the claim say that the “providing” function of the current measuring- and voltage regulating (“CMVR”) circuit must occur during driving of the third transistor’s gate. Defendants’ argument is tortured and incorrect. *See* Flasck Resp. Decl. ¶¶ 9–16.

The term recites “a third thin film transistor during driving its gate” and lists two actions of the third transistor: “taps” and “supplies.” This language is followed by a *comma*, and then a description of the CMVR circuit, which has the function of “providing” a voltage signal. The “during driving its gate” language modifies the third transistor. It does not modify the next clause about the CMVR circuit. This is because modifiers are placed next to the words they modify. *See* William Strunk, Jr. & E.B. White, *The Elements of Style* 30 (4th ed. 2000) (Rule 16). Indeed, the third transistor and CMVR circuit are separated by a comma, which indicates separate clauses. This is confirmed by *Credle v. Bond* case cited in Defendants’ brief. 25 F.3d 1566, 1571 (Fed. Cir. 1994). In *Credle*, the Federal Circuit relied on the placement of commas to construe claim language. *Id.* It found that a comma indicates “the beginning of a new, distinct step to be taken” and that a clause, offset by commas, describes a particular “state of events.” *Id.*

Defendants’ construction is wrong in other ways. The phrase “during driving of [the] gate” appears twice in the claim: (1) when referencing the third transistor and (2) when the OLED is in the “off” state.” But it does not appear in the clause describing the CMVR circuit:

1. A driving circuit for an image point of an image screen which has an organic light-emitting diode, comprising a capacitor; a feedback coupling; a first thin film transistor as a current-driving transistor for the diode; a second transistor which is connected by a current-conducting electrode with a gate of said first transistor and by a second current-conducting electrode with a data conductor and by its gate electrode with a scanning signal conductor; a third thin film transistor which during driving its gate through a driving conductor taps a diode driving current at an output of said first current-driving transistor and supplies a current measuring- and voltage regulating circuit, said current measuring- and voltage regulating circuit providing to the data conductor a voltage signal which is dependent on a current measuring result and a voltage comparison, so that the diode during driving of said gate of said third transistor due to its non-linear switching characteristic acts as a switch for a current deviation in said current measuring- and voltage regulating circuit.

The CMVR clause (highlighted in blue) describes in a general way what the CMVR circuit does, possibly, but not necessarily during the when the third transistor's gate is being driven. Flasck Resp. Decl. ¶ 13. Tellingly, “during driving of its gate” first appears to describe the third transistor and then is *repeated* to describe the diode. It is not mentioned to describe the CMVR circuit. This confirms that the inventors did not intend to limit the claimed “providing” by the CMVR circuit to occur when the third transistor is being driven. *Id.* It also contradicts Defendants’ primary argument that the “during driving its gate” modifies the entire claim language after the last semicolon. If that were true, there would be no need to repeat the language to describe the diode.

Defendants’ cases are inapposite and based on claims with different structure and syntax, such as no separating punctuation. *See* Defs.’ Br. at 17–18. There is no authority that semicolons are the only way to separate a claim and that commas must be ignored. Further, Defendants’ cursory arguments about the specification and figure is unsupported. None of those disclosures say the claimed “providing” by the CMVR circuit must occur while the third transistor’s gate is being driven, and a POSITA would not understand them in this way. Flasck Decl. ¶ 14. To the contrary, the patent teaches that the second and third transistors can be turned on at different times. Thus, a POSITA would understand that the patent contemplates a mode where the claimed “providing” by the CMVR occurs whether or not the third transistor is being driven. *Id.* ¶ 15.

B. “current measuring” (’891 patent claims 1, 3)

Solas’s Proposed Construction	Defendants’ Proposed Construction
No construction necessary (“current measuring”)	measuring <u>actual</u> current (<u>not voltage</u>)

As with the “gradation current” term from the ’137 patent, Defendants’ arguments on this term attack a strawman. Solas wholeheartedly agrees with Defendants that ““current measuring” does not mean ‘voltage measuring.’” Defs. Br., Dkt. 67 at 15. This term requires that a current be

measured. It is not satisfied by something that measures a different physical quantity, like voltage, time, or temperature but does not measure current.

The statements in the specification and in the file history that Defendants cite are fully consistent with—and say nothing beyond what is required by—the claim language itself. They simply say that measurement of a current is required. They do not exclude anything that measures a current, simply because it might also measure something else. Certainly, there is nothing in the specification or file history that meets the standard of “clear and unmistakable” disavowal of some forms of current measurement.

As for the “gradation current” term, Defendants’ negative limitations invite confusion and error. Nothing in the record or in Defendants’ brief explains what it means to be an “actual current” or how such currents differ from any other kind of current. The “(not voltage)” negative limitation risks excluding embodiments that do measure a current, but also measure a voltage or involve a voltage as part of their measurement. Both limitations will improperly place a thumb on the scale and signal to the jury that the Court wants them to apply some narrow, non-standard meaning that differs from the plain and ordinary meaning of “current measuring.”

Moreover, as explained in Solas’s opening brief, Defendants’ proposed construction risks excluding the patent’s preferred embodiment for current measuring, which first converts the current to a voltage and then compares that voltage to a nominal value. Dkt. 68 at 17–18; ’891 patent at Figure, 2:7, 3:17–18, 3:25–26; ’891 IPR Decl., Dkt. 68, Ex. 11, ¶ 76.

Defendants’ construction does not actually define “current measuring” in a way that would help the finder of fact. It simply attempts to insert confusing and legally erroneous negative limitations into an already clear term. These negative limitations should be rejected, and the term should be applied according to its plain and ordinary meaning.

C. **“wherein all above mentioned elements of the driving circuit are located at a same side of said light emitting diode” (’891 patent claim 3)**

Solas’s Proposed Construction	Defendants’ Proposed Construction
wherein all above mentioned elements of the driving circuit <u>are electrically connected to and physically located</u> on the same side of the layers of said light emitting diode	wherein all above mentioned elements of the driving circuit <u>are electrically connected to</u> the anode or cathode of said light emitting diode

The parties agree that claim term includes electrical connection. The only dispute is whether it also includes the physical location of the driving circuit elements. On this point, the claims and specification teach that the purpose of having the driving circuit elements “located on the same side” is to avoid any physical requirement to make vias or contract holes in the OLED organic layers. *See* ’891 cl. 1; 4:41–45, 1:45–50. Further, the specification emphasizes that by locating “all circuit parts at one side of the LED element . . . *a conventional layer sequence can be used during the manufacture.*” *Id.* at 2:28–30. These references to a “conventional layer sequence” and “during manufacture” indicate the term is describing the physical location of elements relative to the layers of the diode. *See* Flasck Resp. Decl. ¶ 17.

The surrounding claim language is also instructive. *See id.* ¶¶ 18–20. The claim states that the circuit elements are located on the same side of the diode “*so that no contacts must be guided through a semiconductor material of the diode.*” *See* ’891 patent, cl. 1. Solas’s construction requiring ***both*** physical location and electrical connection ensures that the condition of “no through holes” is met. Consider four possible scenarios:

P1E1	The circuit elements are physically located on and electrically connected to one side of the diode.
P1E2	The circuit elements are physically located on one side of the diode, but electrically connected to both sides of the diode.

P2E1	The circuit elements are physically located on both sides of the diode, but electrically connected to one side of the diode.
P2E2	The circuit elements are physically located on and electrically connected to both sides of the diode.

Solas’s construction is scenario P1E1. This is the only scenario where the condition of “no through holes” can be met. *See* Flasck Resp. Decl. ¶¶ 20–24. Because the circuitry is physically on one side and all circuit electrical connections go to only one OLED electrode, there is no need to form a contact hole through the OLED layer of the diode.

In contrast, Defendants’ construction includes scenario P2E1. *See id.* In that scenario, the circuit elements are electrically connected to one side of the diode but physically located on both sides of the diode. Importantly, in this scenario, the circuit elements would still be electrically connected to each other. This is illustrated by the ’891 patent figure, which depicts connections between the claimed elements of the driving circuit (e.g., capacitor, feedback coupling, three transistors, and CMVR circuit). Because the elements are physically located on both sides of the diode, a contact hole through the OLED layer must exist to electrically connect a portion of the circuitry on one side of the diode with a portion of the circuitry on the other side. This is true even if the circuit elements only connects with one OLED electrode. Therefore, scenario P1E2 violates the condition that “that no contacts must be guided through a semiconductor material of the diode.”

To ensure the condition that no through holes must exist, all portions of the drive circuit must be both (a) physically be on one side of the diode *and* (b) electrically connected to that side. *See id.* ¶ 25. Defendants’ construction is incomplete and Solas’s construction should be adopted.

Defendants do not point to any disclaimer or lexicography that mandates their construction. The Applicant never redefined “located on” to mean “electrically connected to” as Defendants’ construction would require. *See id.* ¶ 26. For example, the Applicant explained during prosecution

that claim 3 “is not *just about* the physical layers, but about the circuit elements.” ’891 FH at 152–53. This means that the limitation is about *both* physical layering and electrical connections—not “just” about the physical layers.

Nor does the Applicant’s statement that the limitation is “clearly shown in the drawings” operate as a disclaimer. In the same Office Action, the Applicant noted that the “interrelations between a circuit structure and a physically layering are trivial[.]” *Id.* at 153–54. A POSITA would view the circuit diagram in view of the ’891 patent claims and specification, which teach that locating the circuit elements on the same side of the diode is to avoid the necessity of having through holes through the OLED layer and to address problems of manufacturing and product yield. *See* Flasck Resp. Decl. ¶ 26. Thus, the circuit diagram, in context, informs a POSITA that the circuit elements would be physically located on the same side of the diode. *See id.*

III. DISPUTED TERMS FOR ’068 PATENT

A. “formed on said plurality of supply lines along said plurality of supply lines” (’068 patent claim 1) “connected to said plurality of supply lines along said plurality of supply lines” (’068 patent claim 13)

Term	Solas’s Proposed Construction	Defendants’ Proposed Construction
“formed on said plurality of supply lines <i>along</i> said plurality of supply lines”	formed on said plurality of supply lines <u>over the length or direction of</u> said plurality of supply lines	formed on said plurality of supply lines <u>over the length of</u> said plurality of supply lines
“connected to said plurality of supply lines <i>along</i> said plurality of supply lines”	connected to said plurality of supply lines <u>over the length or direction of</u> said plurality of supply lines	connected to said plurality of supply lines <u>over the length of</u> said plurality of supply lines

Defendants are correct that this dispute centers on a single claim term” “along,” used in the claims to describe how the “feed interconnections” are “formed on” or “connected to” the plurality

of “supply lines.” Defendants’ brief, however, does not help their side in this dispute; it only confirms that Solas’s proposed construction is correct. *See* Flasck Decl. ¶¶ 27–36.

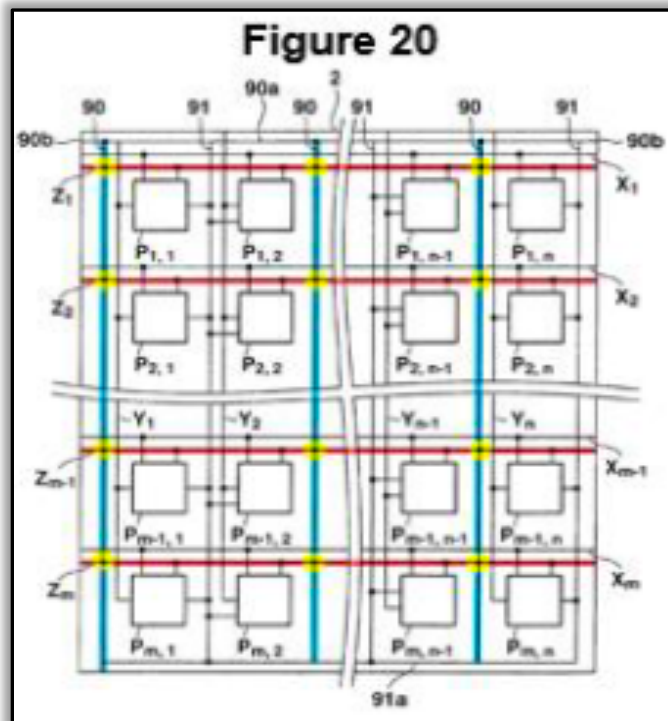
For their part, Defendants never dispute that Solas’s proposed construction—“over the length *or direction of*”—does fall within the plain meaning of the term “along.” Nor could they. Their own dictionary definition cites make clear that *it does*. For example, Defendants quote Webster’s New World College Dictionary to show that “along” must mean “***over and throughout the entire length of***,” as they emphasize on page 22 of their opening brief. But before that emphasized entry, their own dictionary adds the broader, leading definition, which is, “***on or beside the length of***.” This is essentially all Solas seeks to make clear with its proposal to add “or the direction of” to Defendants’ construction—and would be happy this part of Defendants’ own dictionary cite were included in the construction of the term.³

Beyond Defendants’ understandable failure to refute this point about the plain meaning, they advance no argument that the patentee acted as his own lexicographer or unambiguously disclaimed “direction of” or on or besides the length” of from the scope of “along.” That is fatal to their proposed construction—as there is a “heavy presumption” that claim terms carry their “full ordinary and customary meaning, unless [the accused infringer] can show the patentee expressly relinquished claim scope.” *Epistar Corp. v. ITC*, 566 F.3d 1321, 1334 (Fed. Cir. 2009). In other words, Defendants’ construction is narrower than the plain meaning of the phrase—and their refusal to broaden that construction to include the full scope of the term “along” will lead to error. Solas’s construction is the only correct one—and Defendants’ brief makes this clear.

³ And it is consistent with *See* Merriam-Webster (“along: 1: in a line matching ***the length or direction of*** // walking *along* the river; *also*: at a point or points on // a house *along* the river”); Dictionary.com (“along: 1 through, on, beside, over, ***or parallel to the length or direction of***; from one end to the other of: *to walk along a highway*.”).

Instead of presenting any relevant argument against Solas's construction about plain meaning or express relinquishment of claim scope through lexicography or disclaimer, Defendants present three incorrect and legally irrelevant ones. Each fails.

First, unable to contend, let alone show, that the patentee expressly relinquished claim scope through lexicography or disclaimer, Defendants contend their construction reflects “how the inventors use the term in the specification” and that “both” embodiments in the patent support their construction. Defs’ Br. at 21-23. But this argument fails on the facts and the law. On the facts, beyond ignoring plain-meaning definitions in their own dictionaries, Defendants’ proposed construction *does not reflect* “how the inventors use the term in the specification,” but rather *contradicts* the embodiments in the patent. Notably, as Defendants’ own brief shows and states, the so-called “second embodiment” show “[t]he feed interconnections’ (blue) ‘are connected to the supply lines’ (red)” at various intersections “in a grid.” *Id.* at 23. Or as Mr. Flasck explains, “each feed interconnection 90 crosses and connects to each supply line (Z_i) at the crossovers:”



Flasck Resp. Decl. ¶ 31. This embodiment is consistent only with Solas’s construction because the interconnections run “over the length or direction of” the supply lines. They do not, as Defendants’ *construction* might suggest, run just over the length of the supply lines. And they certainly do not, as Defendants’ *possible interpretation of their construction* suggests, run “over and throughout the entire length of” or “for the length of.” *Id.* at 21–22. On the law, of course, this dispute within a dispute is irrelevant anyway. Without clear and unambiguous disclaimer or lexicography, courts “do not import limitations into claims from examples or embodiments appearing only in a patent’s written description, even when a specification describes very specific embodiments of the invention or even describes only a single embodiment.” *See JWW Enters.*, 424 F.3d at 1335.

Second, again avoiding any futile contention that the patentee disclaimed claim scope of acted as his own lexicographer, Defendants argue that the “purpose” of the claim element would be frustrated by Solas’s proposed construction. Defs.’ Br. at 22. Specifically, Defendants suggest that construing the term according to Solas’s proposal—which requires the feed interconnects to exist “over the length or direction of” the supply lines—somehow would not “reduce resistance.” Not so. As Mr. Flasck explains, the patent itself makes clear that the feed interconnects do not need to run the full length of the supply lines to provide some mitigation of the voltage drop problem.—and a POSITA would know this. Flasck Resp. Decl. ¶¶ 35–36. And, as with their first argument, this debate does not matter in the eyes of the Federal Circuit. For their part, Defendants, cite no law holding that this question of supposed “purpose” should decide the claim construction dispute before this Court. There is none, let alone any that would trump the fact that Solas’s construction falls within the undisputable plain meaning of the claim term “along.”

Third, left with little else, Defendants distract from the intrinsic and relevant extrinsic evidence by building a strawman. They contend, in their opening claim construction brief, that

“Solas appears poised to try to use its construction to argue that [its construction] can be satisfied if the feed interconnections merely intersect with the supply lines at any one point even at oblique or orthogonal angles.” Br. at 21. This conclusory attorney argument is wholly unsupported. Indeed, Solas’s construction, “over the length or direction of,” does not support Defendants’ strawman, but rather demonstrably disproves it. This conclusory argument is also legally irrelevant to the issues of claim construction, which must focus on the relevant intrinsic record and relevant extrinsic evidence. *Phillips*, 415 F.3d at 1313–19.

B. “patterned” (’068 patent claims 1, 13)

Solas’s Proposed Construction	Defendants’ Proposed Construction
formed in <u>one or more layers</u>	formed in <u>a single layer</u>

The parties’ only dispute for “patterned” is whether it is necessarily and always limited to a single layer. Defendants’ own descriptions of the term confirm it is not. *See* Defs’ Br. at 25 (‘Patterned’ describes *how different layers* are formed one by one to form the components and lines of the display panel[.]’); Holberg Decl. ¶ 114 (“it’s clear to a POSITA that the ’068 patent uses ‘patterned’ to describe the formation of the display panel *layer by layer*, consistent with its ordinary usage in the art.”). Defendants’ references to “different layers” and “layer by layer” imply that patterning can be applied to a single layer or to multiple layers, such as a stack. Flasck Decl. ¶¶ 116–17; Flasck Resp. Decl. ¶¶ 37–39. Indeed, if “patterned” were restricted to a single layer (under Defendants’ proposed construction), it would not make sense to describe that single layer as being formed “layer by layer.” Flasck Resp. Decl. ¶ 39.

The specification also undermines Defendants’ narrowing construction. Defendants are plain wrong that the specification never uses “patterning” to describe forming more than one layer. *See* Defs.’ Br. at 26. The specification describes patterning a drain layer structure, which can be

“a layered structure including *two or more layers*.” Solas’s Br. at 25–26 (citing ’068 patent at Fig. 8, 9:44–49, 8:47–51). The specification also describes patterning supply lines and scan lines, which can be distinct layers separated by a gate insulating film. *See* ’068 patent at cls. 1, 13, 14 2:52–53, 2:62–65; Flasck Resp. Decl. ¶¶ 40–45.

Defendants’ reliance on the specification’s mentions of “patterning a single conductive film” or “patterning the same material layer” is also misplaced. *See* Defs.’ Br. at 26. The phrases “a single conductive” or “the same material layer” would be redundant if patterning is already limited to a single layer. Indeed, these statements describe a specific type of patterning that is not reflected by the word “patterning” alone. *See Johnson Worldwide Associates, Inc. v. Zebco Corp.*, 175 F.3d 985, 991 (Fed. Cir. 1999) (“Varied use of a disputed term in the written description demonstrates the breadth of the term rather than providing a limited definition.”).

C. “patterned together” (’068 patent claims 1, 13)

Solas’s Proposed Construction	Defendants’ Proposed Construction
patterned <u>to fit together</u>	patterned <u>at the same time</u>

Solas’s construction is consistent with the plain meaning of “together” and the intrinsic and extrinsic evidence. *See* Solas’s Br. at 26–27. A POSITA would understand that in the context of the ’068 patent, elements are “patterned together” if they are in close spatial proximity and designed to fit together in the display panel. *See* Flasck Decl. ¶¶ 120–25; Flasck Resp. Decl. ¶ 41. This is the same understanding reflected in other patents in the art, including the ’722 patent cited in Defendants’ extrinsic evidence disclosure. . The ’722 describes that a “first reflective electrode **294** will be *patterned together* with the second **298** connectors[.]” ’722 patent at 18:32–34.

Elements **294** and **98** are not stacked one upon the other. Flasck Resp. Decl. ¶ 41. It is also clear that **294** and **298** appear as two distinct, laterally separated layers. *Id.* As such, they cannot

be patterned in a single photolithographic step. *Id.* Layers **294** and **296** were patterned at different times with different pattern masks. The reason they are described as “patterned together” is because they are in close spatial proximity and designed to fit together.

Defendants’ construction that “patterned together” means “patterned at the same time” is unsupported⁴ and indeed ***contradicted*** by the ’068 patent. The ’068 claims and specification make clear that (1) the supply lines are “patterned together” with the sources and drains of the driving transistors (’068 patent at cls. 1, 13; 2:52–53); and (2) the scan lines are “patterned together” with the sources and drains (*id.* at cl. 14, 2:62–65). Flasck Resp. Decl. ¶¶ 43. Thus, the patent teaches that the supply lines, scan lines, and transistor sources and drains are all “patterned together.” *Id.*

This contradicts Defendants’ proposed construction because the supply lines and scan lines are in different layers formed at different times. *Id.* ¶¶ 43–44. The ’068 patent teaches that the scan lines cross the supply lines via the gate insulating film. ’068 patent at cl. 14, 2:62–64; Flasck Resp. Decl. ¶¶ 43–44. Thus, at the cross overs, the scan line layer is above the gate insulating layer and the gate insulator layer is above the supply line layer. Flasck Resp. Decl. ¶¶ 43–44. This demonstrates that the supply line layer was patterned ***before*** the gate insulating layer, and that and the gate insulating layer was patterned ***before*** the scan line layer. *Id.*

Thus, the supply lines and scan lines cannot be patterned in a single layer and at the same time as Defendants’ construction would require. *Id.* Defendants’ construction would exclude this embodiment. Such constructions are “rarely, if ever, correct.” *SanDisk Corp.*, 415 F.3d at 1285–86. In contrast, Solas’s construction is consistent with this embodiment because the supply lines

⁴ For example, the specification’s mention of “patterned simultaneously” (Defs.’ Br. at 26) is not about the term “patterned together with,” much less a disclaimer or definition of that term. To the contrary, that the specification uses “patterned simultaneously” supports a broader understanding of patterned. See *Johnson Worldwide*, 175 F.3d 985 at 991 (Fed. Cir. 1999).

and scan lines are in close spatial proximity and designed to fit together in the display panel. Solas's construction should be adopted.

D. "signal lines" ('068 patent claims 1, 13)

Solas's Proposed Construction	Defendants' Proposed Construction
conductive lines supplying signals	conductive lines supplying <u>a value corresponding to a luminance level</u>

Defendants suggest that Solas's construction is improper because it would encompass conductive lines "carrying *any* signal" rather than just lines carrying specific types of signals. Defs.' Br., Dkt. 67 at 27. Defendants' argument misses the mark.

What the patentee claimed was "signal lines," not signal lines carrying specific types of signals. Accordingly, there is a "heavy presumption" that the claim terms cover the "full ordinary and customary meaning" of "signal lines." *Epistar Corp. v. ITC*, 566 F.3d 1321, 1334 (Fed. Cir. 2009). Defendants fail to cite any evidence of lexicography or of clear and unmistakable disavowal that would support narrowing "signal lines" from their plain and ordinary meaning.

Defendants point to the fact that the claims also refer to other types of "lines," such as "supply lines" and "scan lines." That may suggest that "signal lines" does not mean exactly the same thing as "supply lines" or as "scan lines," but it does not mean that they must be construed as mutually exclusive terms and does not justify narrowing "signal lines" to specific embodiments from the specification. Indeed, both sides' constructions for "signal lines" describes them as "supplying" something, so both sides propose constructions that suggest that "signal lines" and "supply lines" might overlap at least to some degree.

The only other support that Defendants cite for their construction from the intrinsic record is the discussion of what "signal lines" do in "conventional" prior art devices or in specific

preferred embodiments. None of these statements purports to define “signal lines” or in any way disavows the use of other types of signal line in the invention.

Defendants’ effort to import “luminance level” as a limitation into the claims is particularly inappropriate for claim 1. Claim 1 claims a “transistor array substrate” and never expressly mentions displays, pixels, or emitting light. Defendants’ proposed construction would effectively require that the transistor array substrate of claim 1 be used to emit light in an array of pixels, contrary to the plain meaning of the claim.

Defendants’ effort to import limitations from prior art or from the preferred embodiments should be rejected, and Solas’s construction, grounded in the plain meaning of the term in the context of the claims should be adopted

E. “feed interconnections” (’068 patent claims 1, 10, 12, 13, 17)

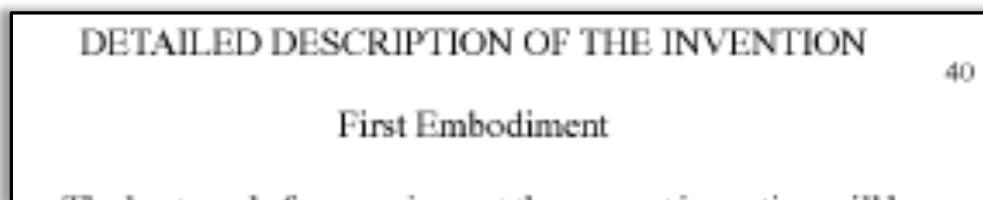
Solas’s Proposed Construction	Defendants’ Proposed Construction
conductive structures in a layer or layers that provide connections to a source that supplies voltage and/or current	conductive structures in a layer or layers <u>different from the gates, sources and drains</u> that provide connections to a source that supplies voltage and/or current

The plain meaning of “interconnections” in the context of the ’068 patent is a conductive structure in a layer or layers that provides electrical connections between two circuit elements. Flasck Decl. ¶¶ 132–33. As the overlap between the two competing constructions makes clear, the parties essentially agree on this point.

The parties’ competing constructions also confirm agreement that the “feed interconnections” species of connections provides connections to “a source that supplies voltage and/or current.” As Mr. Flasck and other evidence makes clear, this is part of the plain and ordinary meaning of the disputed term, in light of the intrinsic evidence. *See id.* And Solas’s construction should be adopted. *Id.*

Defendants’ contrary arguments are based on the false premise that “the very character of the inventions” in the patent requires a construction that further limits the term to one in which the conductive structures are in a layer that is “different from the gates, sources, and drains.” Defs’ Br. at 29–30. But the intrinsic evidence just does not support this take; Flasck Resp. Decl. ¶ 46.

To the contrary, in support of this false premise, Defendants cite only two parts of the patent specification—and neither supports Defendants’ premise. The first citation is to a part of the “Summary of the Invention,” that expressly describes an “aspect” or embodiment of the inventions—and only for “*a panel according to claim 13*,”—the feed interconnection are “formed separately for the drains, sources, and gates of the driving transistors.” 2:39-4:09. And even then, it is merely done in accordance with what the patentee “[p]referably” teaches for Claim 13. Defendants’ second citation fares no better. Like the first, it merely points to one aspect of one embodiment of the patent, described at column 18, lines 26-40. But even a cursory review of that column of the specification makes clear that this is just one preferred aspect of just one embodiment. Indeed, zooming out of that “aspect” proves that the entire section it falls under is only the “First Embodiment” of the invention (at 5:38–42):



This record makes this case very different from Defendants’ cited cases—and under any reasonable view, neither of Defendants’ citations comes close to amounting to a description of “the very character of the inventions.” If anything, the fact that they describe only one of several embodiments actively disproves the premise. Even if we ignore the other embodiments past the first one, controlling law still cuts against Defendants’ premise. Without clear and unambiguous

disclaimer or lexicography, courts “do not import limitations into claims from examples or embodiments appearing only in a patent’s written description, even when a specification describes very specific embodiments of the invention or even describes only a single embodiment.” *See JWW Enters.*, 424 F.3d at 1335.

In other words, Defendants’ importation is not “preferabl[e],” let alone required, in the other embodiments beyond the “first” one. And consequently, leaving it out of the construction for all claims would not frustrate “the object of the present invention,” as Defendants wrongly suggest. Indeed, even accepting that an object of the present invention is to “satisfactorily drive a light-emitting element while suppressing any voltage drop and signal delay,” as Mr. Flasck explains, that “object” can and would be achieved by the claimed invention *regardless* of whether it is limited in the way Defendants contend it should be. Flasck Resp. Decl. ¶ 48.

Dated: April 3, 2020

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ATTORNEYS FOR PLAINTIFF,
SOLAS OLED LTD.

CERTIFICATE OF SERVICE

I certify that on April 3, 2020, all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system pursuant to Local Rule CV-5(a)(3)(A).

/s/ Neil A. Rubin
Neil Rubin